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(54) **Semiconductor device with a fusible link and method of making a fusible link on a semiconductor substrate**

Halbleitervorrichtung mit schmelzbarer Verbindung und Verfahren zum Herstellen einer schmelzbaren Verbindung auf einem Halbleitersubstrat

Dispositif semiconducteur avec une liaison fusible et procédé de fabrication d'une liaison fusible sur un substrat semiconducteur

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- **RESEARCH DISCLOSURE, no. 264, April 1986, pages 202-203, Emsworth, Hampshire, GB; "Programmable fuse utilizing deposited conformal metal stringers as the fuse element"**
- **PATENT ABSTRACTS OF JAPAN, vol. 8, no. 235 (E-275)[1672], 27th October 1984; & JP-A-59 117 157**

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Description

Background of the Invention

This invention relates, in general, to semiconductor devices with fusible links, and to a method of making fusible links on a semiconductor substrate.

Memory elements are used in integrated circuit memory devices, such as Programmable Array Logic devices (PAL's), Programmable Logic Array devices (PLA's), or Programmable Read Only Memories (PROM's) to produce field programmable products. Memory elements can be horizontal, metallic, fusible links; transistors which are shorted when sufficient reverse current is supplied; or floating gate transistors which can be turned on and off by introducing and releasing charge on the gate.

Metallic fusible links are typically employed in high performance applications using bipolar/BICMOS technologies. In a memory array, a transistor supplies sufficient current to blow the fusible link to create an open circuit between a selected pair of bit and word lines. Fusible links remain intact to represent one logic state, and are fused open to represent the opposite logic state. The amount of energy required for fusing open a fusible link is determined primarily by the fusible link cross-sectional area in the fusing portion. Other parameters which affect the amount of energy required for fusing are the resistivity, thermal conductivity, and melting temperature of the fusible link material.

In the past, fusible links have been fabricated by using a thin, horizontal, conductive or semiconductive film of either polysilicon, nickel chrome, platinum silicide, or titanium tungsten. A disadvantage of fabricating the fusible links in this manner is that a high fusing power is required for fusing. This means that larger transistors and diodes must be provided to handle the larger currents. The fusing power required can not be significantly reduced because a reduction of the fusible link cross-sectional area is limited. The thickness of the fusible link material is typically on the order of 100nm (1000 Angstrom). The width of the link is on the order of 2 microns and can not be reduced due to photolithography constraints.

Thus, there is a need to provide a means of fabricating a fusible link having a smaller cross-sectional area than can be defined by the method described above. A fusible link having a smaller cross-sectional area will require a lower fusing power. Smaller transistors and diodes can be used, thereby reducing the die size of the integrated circuit memory device.

An article entitled "Programmable Fuse Utilizing Deposited Conformal Metal Stringers as the Fuse Element" in Research Disclosure, no. 264, April 1986, pages 202-203, Emsworth, Hampshire, GB describes a technique for making in-chip fuses in wafers. The technique utilises etching and masking steps to form undercut sidewalls. The undercut regions are then filled with conformal metal to form a fuse.

Summary of the Invention

According to a first aspect of the present invention , there is provided a method of making a fusible link on a semiconductor substrate, comprising the steps of:

providing a dielectric layer on the semiconductor substrate;
patterning a platform or a well from the dielectric layer having substantially vertical sidewalls;
forming a layer of a fusible material over and around the platform or well, the fusible material consisting of a conductive or semiconductive material;
etching the layer of fusible material to leave a fusible sidewall spacer along a sidewall of the platform or well; and
forming first and second electrodes contacting the fusible sidewall spacer at opposite ends thereof, whereby the fusible sidewall spacer forms a fusible link therebetween which is fusible by an electric current.

In accordance with a second aspect of the present invention there is provided a semiconductor device comprising:

a semiconductor substrate, a dielectric layer located on the substrate a well or a platform formed in the surface of the dielectric layer providing a substantially vertical sidewall, a fusible sidewall spacer formed along the sidewall, said fusible sidewall spacer being formed from a conductive material or a semiconductive material, and a first electrode and a second electrode, the first and second electrodes contacting the fusible sidewall spacer at opposite ends thereof, whereby the fusible sidewall spacer forms a fusible link therebetween which is fusible by an electric current.

Another disadvantage of the fusible links made in the past is that a defect in the fusible link may cause the link to be open. Thus, there is also a need to provide a fusible link having a built-in redundancy. Built-in redundancy could provide two separate fusible portions in one fusible link element, so that if there is a defective portion on the fusible link, an intact fuse state is still formed.

It is preferred that the well or platform has a quadrilateral shape and has sidewalls extending around the well or the platform and wherein the fusible sidewall spacer extends round all the sidewalls of the well or platform and wherein the first electrode is in electrical contact with first ends of two opposing sides of the sidewall spacer and wherein the second electrode is in electrical contact with second ends of the two opposing sides of the sidewall spacer, such that the two opposing sides of the sidewall spacer form two fusible links between the electrodes.

Thus, an improved fusible link is provided requiring lower fusing power and a built-in redundancy.

The method of fabricating has the advantage of providing a fusible link having a small cross-sectional area, thus requiring low fusing power.

The method is compatible with modern bipolar and BICMOS processes.

The fusible link preferably has built-in redundancy by fabricating the fusible link with two fusible portions per site.

The invention allows for increased packing density of fusible links on an integrated circuit area.

Brief Description of the Drawings

Figs 1-2 illustrate enlarged cross-sectional views of a structure embodying the present invention in various stages of development;

Fig 3 illustrates an enlarged top view of a structure embodying the present invention; and

Fig 4 illustrates an enlarged cross-sectional view of a second embodiment of the present invention.

Figs 1-3 illustrate one embodiment of the present invention in various stages of development. Fig 1 illustrates a semiconductor substrate 10 with a dielectric layer 11 deposited thereon. Substrate 10 will have semiconductor devices built therein, however, they are not illustrated here. A second dielectric layer 12 is deposited on layer 11 and then patterned to leave a transition or platform 12. Dielectric layer 11 and 12 can be comprised of two different dielectrics having an interface at dotted line 16. Dielectric layers 11 and 12 can also be comprised of a single dielectric layer which is patterned to form a platform 12. In a preferred embodiment, dielectric layers 11 and 12 would be a single layer of oxide, however, dielectric layers 11 and 12 can be any combination of oxide, nitride, or the like. A fusible layer 13 is then formed on dielectric layers 11 and 12. A fusible layer 13 is made of a conductive or semiconductive material such as doped polysilicon, silicided polysilicon, or a metal. Dielectric layers 11 and 12, and fusible layer 13 are deposited by any standard processes known in the art.

Fig 2 illustrates the structure of Fig 1 with fusible layer 13 partially etched to form a fusible sidewall spacer 13. Layer 13 is etched in the same manner that is used to form a dielectric sidewall spacer. In a preferred embodiment, fusible sidewall spacer 13 is formed by employing a directional etch, such as a Reactive Ion Etch (RIE), that only etches in the vertical direction. In addition, a combination of a vertical and a horizontal etch may be used as long as fusible sidewall spacer 13 is not completely removed. Sidewall spacer technology is common in bipolar and BICMOS integrated circuit processes. Typically, sidewall spacers are dielectric spacers used to isolate two electrodes by a submicron distance. In the present invention, layer 13 is not a dielectric layer, but a conductive or semiconductive layer which is fusible. Since sidewall spacer technology is commonly used in bipolar and BICMOS processes, the process illustrated here can be easily integrated into the structure shown.

As one can note from Fig 2, the cross-sectional area of fusible sidewall spacer 13 is very small. Photolithography does not limit the width of fusible sidewall spacer 13 as in the prior art. In the present invention, the thickness and the width can both be on the order of approximately 100 nm (1000 Angstrom). The small cross-sectional area results in low power required to fuse open a fusible link made with a fusible sidewall spacer 13 and can still facilitate low fuse resistances by virtue of proper choice of materials. The present invention allows for more flexibility in choosing a conductive or semiconductive layer 13 having a higher melting temperature, because the cross-sectional area can be greatly reduced.

Fig 3 illustrates the structure of Fig 2 from a top view. The structure is also illustrated having two electrodes 14 and 15 making electrical contact to fusible sidewall spacer 13. As one can note from Fig 3, a fusible link is formed having two fusible portions per site, thereby providing for a built-in redundancy. If one portion of fusible sidewall spacer 13 is defective, the other portion can still be fused open or left intact. If there are no defects, both portions will fuse. A fusible link may also be fabricated without having a built-in redundancy, if desired, by providing four electrodes (not illustrated), instead of only two electrodes 14 and 15, making contact to fusible sidewall spacer 13. In this manner, up to four fusible links can be provided by using each side of fusible sidewall spacer 13 as a fusible link. Thus, the packing density of fusible links on a given semiconductor device area can be increased substantially.

Fig 4 illustrates a second embodiment of the present invention. Dielectric layers 11 and 12 are deposited on substrate 10 and a fusible sidewall spacer 13 is fabricated thereon as in Figs 1 and 2. Fig 4 is very similar to Fig 2 except that fusible sidewall spacer 13 is formed inside a transition that is a well in dielectric layers 11 and 12 rather than on a platform as in Fig 1. Furthermore, dielectric layers 11 and 12 can be comprised of two different dielectric layers having an interface at dotted line 16, or a single dielectric layer as described in Fig 1.

By now it should be appreciated that there has been provided a new and improved method of fabricating a fusible link element which is compatible with modern bipolar and BICMOS processes.

Claims

1. A method of making a fusible link on a semiconductor substrate (10), comprising the steps of:

   providing a dielectric layer (11) on the semiconductor substrate (10);

   patterning a platform or a well (12) from the dielectric layer (11) having substantially vertical sidewalls;

forming a layer of a fusible material over and around the platform or well (12), the fusible material consisting of a conductive or semiconductive material;
etching the layer of fusible material (13) to leave a fusible sidewall spacer along a sidewall of the platform or well (12); and
forming first (14) and second (15) electrodes contacting the fusible sidewall spacer at opposite ends thereof, whereby the fusible sidewall spacer forms a fusible link therebetween which is fusible by an electric current.

2. The method of claim 1 wherein the material from which the fusible sidewall spacer (13) is formed is selected from the group of polysilicon, doped polysilicon or silicided polysilicon.

3. The method according to any preceding claim wherein the patterning step comprises patterning a well or platform having a quadrilateral shape and sidewalls extending around the well or platform, wherein the etching a fusible sidewall spacer step comprises forming a fusible sidewall spacer extending round all the sidewalls of the well or platform, and wherein the step of forming first and second electrodes comprises:

forming the first electrode (14) in electrical contact with first ends of two opposing sides of the sidewall spacer; and
forming the second electrode (15) in electrical contact with second ends of the two opposing sides of the sidewall spacer, whereby the two opposing sides of the sidewall spacer form two fusible links between the electrodes.

4. A semiconductor device comprising:
a semiconductor substrate (10), a dielectric layer (11) located on the substrate, a well (12) or a platform (12) formed in the surface of the dielectric layer providing a substantially vertical sidewall, a fusible sidewall spacer (13) formed along the sidewall, said fusible sidewall spacer being formed from a conductive material or a semiconductive material, and a first electrode (14) and a second electrode (15), the first (14) and second (15) electrodes contacting the fusible sidewall spacer at opposite ends thereof, whereby the fusible sidewall spacer forms a fusible link therebetween which is fusible by an electric current.

5. A device according to claim 4, wherein the well or platform has a quadrilateral shape and has sidewalls extending around the well or the platform and wherein the fusible sidewall spacer extends round all the sidewalls of the well or platform and wherein the first electrode (14) is in electrical contact with first ends of two opposing sides of the sidewall spacer and wherein the second electrode (15) is in electrical contact with second ends of the two opposing sides of the sidewall spacer, such that the two opposing sides of the sidewall spacer form two fusible links between the electrodes.

Patentansprüche

1. Ein Verfahren zur Herstellung einer schmelzbaren Verbindung auf einem Halbleitersubstrat (10), das die Schritte umfaßt:

Bereitstellten einer dielektrischen Schicht (11) auf dem Halbleitersubstrat (10);

Erzeugen eines Musters einer Plattform oder einer vertiefung (12) von der dielektrischen Schicht (11), die im wesentlichen vertikale Seitenwände aufweist;

Bilden einer Schicht aus einem schmelzbaren Material über der und um die Plattform oder die Vertiefung (12) herum, wobei das schmelzbare Material aus einem leitenden oder halbleitenden Material besteht;

Ätzen der Schicht aus schmelzbarem Material (13), um ein schmelzbares Seitenwandabstandsteil entlang eine Seitenwand der Plattform oder der Vertiefung (12) zurückzulassen; und

Bilden einer ersten (14) und zweiten (15) Elektrode, die mit dem schmelzbaren Seitenwandabstandsteil an entgegengesetzten Enden davon in Kontakt sind, wodurch das schmelzbare Seitenwandabstandsteil eine schmelzbare Verbindung dazwischen bildet, die durch einen elektrischen Strom schmelzbar ist.

2. Das Verfahren des Anspruchs 1, worin das Material, aus dem das schmelzbare Seitenwandabstandsteil (13) gebildet ist, aus der Gruppe aus Polysilicium, dotiertem Polysilicium oder Silicid-Polysilicium (silicided polysilicium) ausgewählt ist.

3. Das verfahren gemäß irgendeinem der vorhergehenden Ansprüche, worin der Mustererzeugungsschritt umfaßt, ein Muster einer Vertiefung oder einer Plattform herzustellen, die eine vierseitige Form und Seitenwände hat, die sich um die Vertiefung oder die Plattform herum erstrecken, worin der Schritt zum Ätzen eines schmelzbaren Seitenwandabstandsteils umfaßt, ein schmelzbares Seitenwandabstandsteil zu bilden, das sich um alle Seitenwände der vertiefung oder Plattform herum er-

streckt, und worin der Schritt des Bildens einer ersten und zweiten Elektrode umfaßt:

Bilden der ersten Elektrode (14) in elektrischem Kontakt mit ersten Enden zweier entgegengesetzter Seiten des Seitenwandabstandsteils; und

Bilden der zweiten Elektrode (15) in elektrischem Kontakt mit zweiten Enden der zwei entgegengesetzten Seiten des Seitenwandabstandsteils, wodurch die zwei entgegengesetzten Seiten des Seitenwandabstandsteils zwei schmelzbare Verbindungen zwischen den Elektroden bilden.

4. Eine Halbleitereinrichtung, umfassend:
ein Halbleitersubstrat (10), eine dielektrische Schicht (11), die sich auf dem Substrat befindet, eine Vertiefung (12) oder eine Plattform (12), die in der Oberfläche der dielektrischen Schicht gebildet sind und eine im wesentlichen senkrechte Seitenwand aufweist, ein schmelzbares Seitenwandabstandsteil (13), das entlang der Seitenwand gebildet ist, wobei das genannte schmelzbare Seitenwandabstandsteil aus einem leitenden Material oder einem Halbleitermaterial gebildet ist, und eine erste Elektrode (14) und eine zweite Elektrode (15), wobei die erste (14) und zweite (15) Elektrode mit dem schmelzbaren Seitenwandabstandsteil an entgegengesetzten Enden davon in Kontakt sind, wodurch das schmelzbare Seitenwandabstandsteil eine schmelzbare Verbindung dazwischen bildet, die durch einen elektrischen Strom schmelzbar ist.

5. Eine Einrichtung gemäß Anspruch 4, worin die Vertiefung oder die Plattform eine vierseitige Form hat und Seitenwände hat, die sich um die Vertiefung oder die Plattform herum erstrecken und worin sich das schmelzbare Seitenwandabstandsteil über alle Seitenwände der Vertiefung oder der Plattform erstreckt, und worin die erste Elektrode (14) in elektrischem Kontakt mit ersten Enden von zwei entgegengesetzten Seiten des Seitenwandabstandsteils ist, und worin die zweite Elektrode (15) in elektrischem Kontakt mit den zweiten Enden der zwei entgegengesetzten Seiten des Seitenwandabstandsteils ist, so daß die zwei entgegengesetzten Seiten des Seitenwandabstandsteils zwei schmelzbare Verbindungen zwischen den Elektroden bilden.

Revendications

1. Procédé d'élaboration d'une liaison fusible sur un substrat semiconducteur (10), comprenant les étapes de :
fourniture d'une couche diélectrique (11) sur le substrat semiconducteur (10) ;
modélisation d'une plate-forme ou d'un puits (12) à partir d'une couche diélectrique (11) ayant des parois latérales sensiblement verticales ;
formation d'une couche de matériau fusible sur et autour de la plate-forme ou du puits (12), le matériau fusible étant composé d'un matériau conducteur ou semiconducteur ;
attaque de la couche de matériau fusible (13) pour laisser une pièce d'écartement de paroi latérale fusible le long d'une paroi latérale de la plate-forme ou du puits (12) ; et
formation d'une première (14) et d'une deuxième (15) électrodes établissant un contact avec la pièce d'écartement de la paroi latérale fusible aux extrémités opposées de celle-ci, la pièce d'écartement de la paroi latérale fusible formant ainsi une liaison fusible entre les deux qui peut être fondue à l'aide d'un courant électrique.

2. Procédé selon la revendication 1, dans lequel le matériau à partir duquel la pièce d'écartement de la paroi latérale fusible (13) est élaborée est choisi dans le groupe composé de polysilicium, de polysilicium dopé ou de polysilicium silicé.

3. Procédé selon l'une quelconque des revendications précédentes, dans lequel l'étape de modélisation comprend la modélisation d'un puits ou d'une plate-forme ayant une forme de quadrilatère et des parois latérales qui s'étendent autour du puits ou de la plate-forme, dans lequel l'étape d'attaque d'une pièce d'écartement de la paroi latérale fusible comprend la formation d'une pièce d'écartement de la paroi latérale fusible s'étendant autour de toutes les parois latérales du puits ou de la plate-forme, et dans lequel l'étape de formation des première et deuxième électrodes comprend :

la formation de la première électrode (14) qui doit être en contact électrique avec les premières extrémités des deux côtés opposés de la pièce d'écartement de la paroi latérale ; et
la formation de la deuxième électrode (15) qui doit être en contact électrique avec les deuxièmes extrémités des deux côtés opposés de la pièce d'écartement de la paroi latérale, les deux côté opposés de la pièce d'écartement de la paroi latérale formant ainsi deux liaisons fusibles entre les électrodes.

4. Dispositif à semiconducteur comprenant :
un substrat semiconducteur (10), une couche diélectrique (11) située sur le substrat, un puits (12) ou une plate-forme (12) formée sur la surface de la

couche diélectrique fournissant une paroi latérale sensiblement verticale, une pièce d'écartement de la paroi latérale fusible (13) formée le long de la paroi latérale, ladite pièce d'écartement de la paroi latérale fusible étant formée à partir d'un matériau conducteur ou d'un matériau semiconducteur, et une première électrode (14) et une deuxième électrode (15), la première (14) et la deuxième (15) électrodes établissant un contact avec la pièce d'écartement de la paroi latérale fusible aux extrémités opposées de celui-ci, la pièce d'écartement de la paroi latérale fusible formant ainsi une liaison fusible entre les deux qui peut être fondue à l'aide d'un courant électrique.

5. Dispositif selon la revendication 4, dans lequel le puits ou la plate-forme présente une forme de quadrilatère et présente des parois latérales qui s'étendent autour du puits ou de la plate-forme et dans lequel la pièce d'écartement de la paroi latérale fusible s'étend autour de toutes les parois latérales du puits ou de la plate-forme et dans lequel la première électrode (14) est en contact électrique avec les premières extrémités de deux côtés opposés de la pièce d'écartement de la paroi latérale et dans lequel la deuxième électrode (15) est en contact électrique avec les deuxièmes extrémités des deux côtés opposés de la pièce d'écartement de la paroi latérale, de sorte que les deux côtés opposés de la pièce d'écartement de la paroi latérale forment deux liaisons fusibles entre les électrodes.

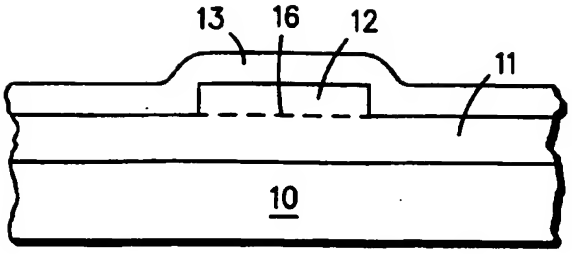

FIG. 1

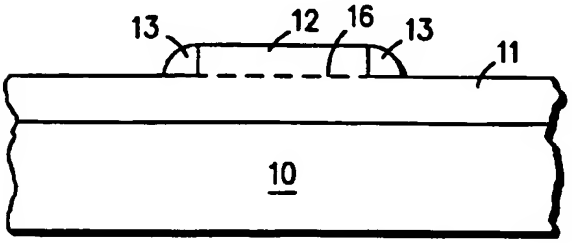

FIG. 2

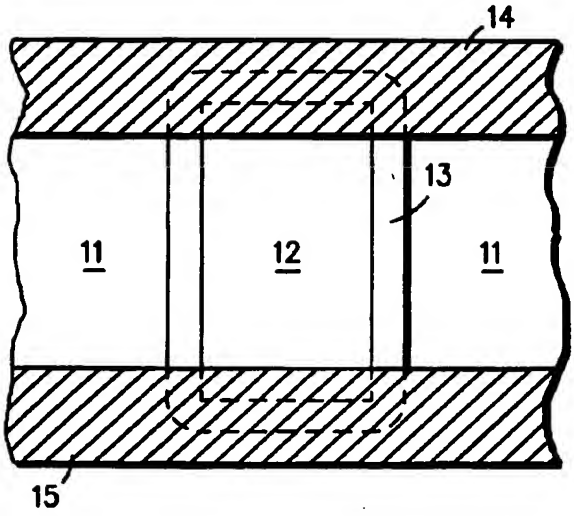

FIG. 3

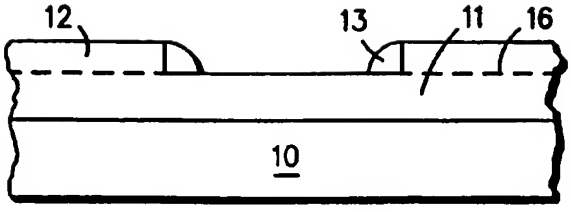

FIG. 4